SODIMM DDR4 3200 4GB Datasheet

(SQR-SD4N4G3K2MNPEA)

Features:

- **Compliance with**
  - RoHS compliant products.
  - JEDEC standard 1.2V ± 0.06V power supply
  - VDDQ=1.2V ± 0.06V
  - Clock Freq: 1600MHz for 3200Mb/s/Pin.
  - Programmable CAS Latency: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 24
  - Programmable /CAS Write Latency (CWL) = 16, 20(DDR4-3200)
  - 8 bit pre-fetch
  - Burst Length: 4, 8
  - Bi-directional Differential Data-Strobe
  - On Die Termination with ODT pin
  - Serial presence detect with EEPROM
  - Asynchronous reset
  - 30 u" PCB golden finger thickness
  - Embedded Anti-sulfur resistor
  -
- **SDRAM Configuration:** DDR4 8Gb 512Mx16 SDRAM
- **Capacities**

  4GB 512Mx64 1 Rank
- **Performance**
  - DDR4-3200 PC4-25600 CL22
- **DRAM Type**
  - DDR4 SODIMM
- **Temperature ranges**

Operating:

  - Nonindustrial: 0°C to 85°C
- **Supply voltage**
  - V_{DD}=V_{DDQ}=1.2 Volt
  - V_{DDSPD}=1.7V~3.6V

    (T_{CASE}: 0°C to 85°C)
- **Form factor**
  - DDR4 260 Pin SODIMM
- **Certification and Compliance**
  - RoHs
  - REACH
  - CE
  - FCC

Revision History:

Rev.	Description	Date
1.0	Official release	2021/05/03
1.1	Revised Format	2021/05/17
1.2	Revised Format	2021/05/26

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1. ADVANTECH Memory Product Description

1.1 Introduction

ADVANTECH Unbuffered Small Outline DDR4 SDRAM DIMMs (Unbuffered Small Outine Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are high-speed operation memory modules that use DDR4 SDRAM devices. These DDR4 SDRAM Unbuffered Small Outline DIMMs are intended for use as main memory when installed in systems such as micro servers and mobile personal computers.

1.2 Key Parameter

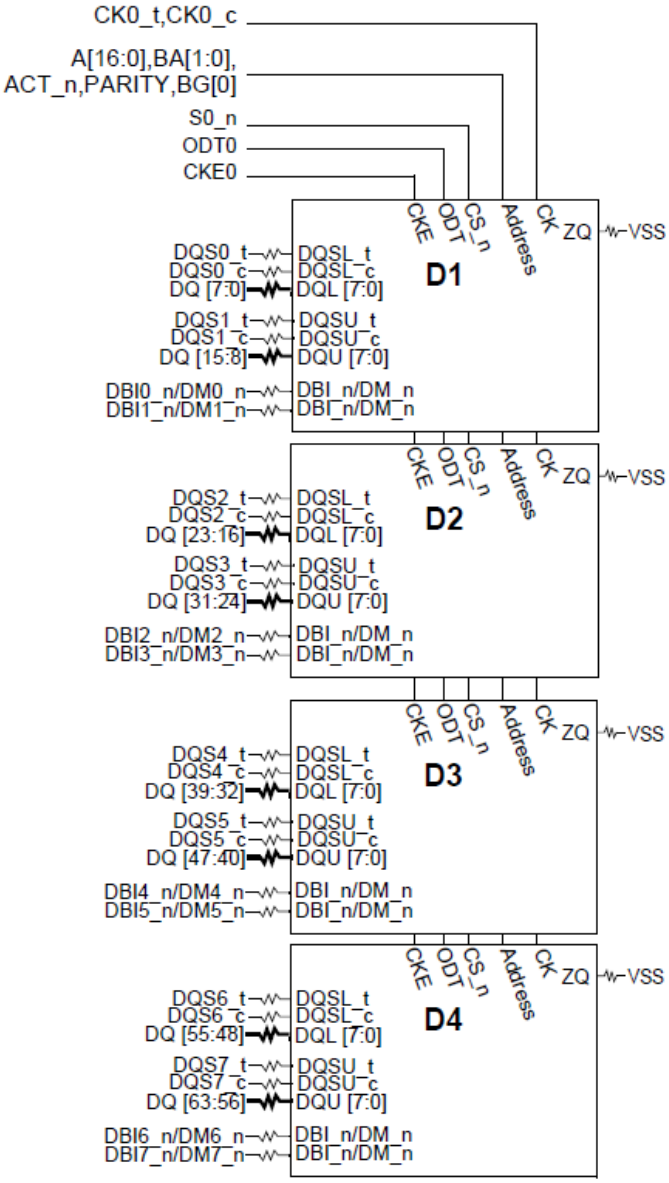
Industry Nomenclature	Data Rate MT/s CL=22	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)
PC4-25600	3200	13.75	13.75	32	45.75

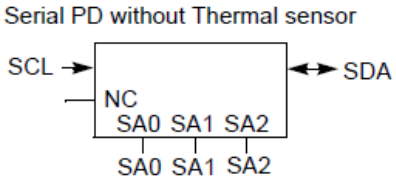
1.3 Ordering Information

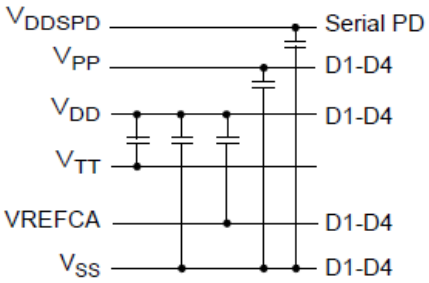
DDR4 SODIMM					
Part Number	Capacity	Speed	DIMM Organization	Number of DRAM	Number of rank
SQR-SD4N4G3K2MNPEA	4GB	PC4-25600	512Mx64	4	1

2. ADVANTECH Memory Module Block Diagram

- DDR4 4GB, 512Mx16 base, 1Rank







3. Environment Requirement

3.1.ADVANTECH DIMM Parameter

ADVANTECH DIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature	0 to +85	°C	1),2)
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	3)

Note:

1) Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

2) At 0° C - 85° C, operation temperature range are the temperature which all DRAM specification will be supported.

3) Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3.2.SDARM parameter by device density

RTT_Nom Setting	Parameter		8Gb	Units
tREFI	Average periodic refresh interval	0°C≦TCASE≦85°C	7.8	μs

4. Absolute Maximum Rating

4.1.Module Absolut Maximum Rating

Symbol	Parameter	Rating	Units	Notes
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.3 to +1.5	V	1)
V_{DD}	Voltage on VDD relative to Vss	-0.3 to +1.5	V	1)
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.3 to +1.5	V	1)

Note:

1) Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4.2.SDRAM Absolut Maximum Rating

Symbol	Parameter	Rating	Units	Note
T_{OPER}	Operation Temperature	0 to 85	℃	1), 2)
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss	-0.3 to +1.5	V	3)
V_{DD}	Voltage on VDD supply relative to Vss	-0.3 to +1.5	V	3)
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.3 to +1.5	V	3)

Note:

1) Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

2) At 0°C - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

3) Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Pin Configurations (Front side/Back side)

5.1.Pin Assignment

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VSS	89	VSS	177	DQS4_c	02	VSS	90	VSS	178	DM4_n, DBI4_n,NC
03	DQ5	91	CB1/NC	179	DQS4_t	04	DQ4	92	CB0/NC	180	VSS
05	VSS	93	VSS	181	VSS	06	VSS	94	VSS	182	DQ39
07	DQ1	95	DQS8_c	183	DQ38	08	DQ0	96	DM8_n, DBI_n,NC	184	VSS
09	VSS	97	DQS8_t	185	VSS	10	VSS	98	VSS	186	DQ35
11	DQS0_c	99	VSS	187	DQ34	12	DM0_n, DBI0_n,NC	100	CB6/NC	188	VSS
13	DQS0_t	101	CB2/NC	189	VSS	14	VSS	102	VSS	190	DQ45
15	VSS	103	VSS	191	DQ44	16	DQ6	104	CB7/NC	192	VSS
17	DQ7	105	CB3/NC	193	VSS	18	VSS	106	VSS	194	DQ41
19	VSS	107	VSS	195	DQ40	20	DQ2	108	RESET_n	196	VSS
21	DQ3	109	CKE0	197	VSS	22	VSS	110	CKE1	198	DQS5_c
23	VSS	111	VDD	199	DM5_n, DBI5_n,NC	24	DQ12	112	VDD	200	DQS5_t
25	DQ13	113	BG1	201	VSS	26	VSS	114	ACT_n	202	VSS
27	VSS	115	BG0	203	DQ46	28	DQ8	116	ALERT_n	204	DQ47
29	DQ9	117	VDD	205	VSS	30	VSS	118	VDD	206	VSS
31	VSS	119	A12	207	DQ42	32	DQS1_c	120	A11	208	DQ43
33	DM1_n, DBI_n,NC	121	A9	209	VSS	34	DQS1_t	122	A7	210	VSS
35	VSS	123	VDD	211	DQ52	36	VSS	124	VDD	212	DQ53
37	DQ15	125	A8	213	VSS	38	DQ14	126	A5	214	VSS
39	VSS	127	A6	215	DQ49	40	VSS	128	A4	216	DQ48
41	DQ10	129	VDD	217	VSS	42	DQ11	130	VDD	218	VSS
43	VSS	131	A3	219	DQS6_c	44	VSS	132	A2	220	DM6_n, DBI6_n,NC
45	DQ21	133	A1	221	DQS6_t	46	DQ20	134	EVENT_n	222	VSS
47	VSS	135	VDD	223	VSS	48	VSS	136	VDD	224	DQ54
49	DQ17	137	CK0_t	225	DQ55	50	DQ16	138	CK1_t	226	VSS
51	VSS	139	CK0_c	227	VSS	52	VSS	140	CK1_c	228	DQ50

53	DQS2_c	141	VDD	229	DQ51	54	DM2_n/ DBI2_n,NC	142	VDD	230	VSS
55	DQS2_t	143	PARITY	231	VSS	56	VSS	144	A0	232	DQ60
57	VSS	145	BA1	233	DQ61	58	DQ22	146	A10/AP	234	VSS
59	DQ23	147	VDD	235	VSS	60	VSS	148	VDD	236	DQ57
61	VSS	149	CS0_n	237	DQ56	62	DQ18	150	BA0	238	VSS
63	DQ19	151	WE_n/ A14	239	VSS	64	VSS	152	RAS_n/ A16	240	DQS7_c
65	VSS	153	VDD	241	DM7_n,DBI7_n,NC	66	DQ28	154	VDD	242	DQS7_t
67	DQ29	155	ODT0	243	VSS	68	VSS	156	CAS_n/ A15	244	VSS
69	VSS	157	CS1_n	245	DQ62	70	DQ24	158	A13	246	DQ63
71	DQ25	159	VDD	247	VSS	72	VSS	160	VDD	248	VSS
73	VSS	161	ODT1	249	DQ58	74	DQS3_c	162	C0, CS2_n,NC	250	DQ59
75	DM3_n, DBI3_n,NC	163	VDD	251	VSS	76	DQS3_t	164	VREFCA	252	VSS
77	VSS	165	C1, CS3_n, NC	253	SCL	78	VSS	166	SA2	254	SDA
79	DQ30	167	VSS	255	VDDSPD	80	DQ31	168	VSS	256	SA0
81	VSS	169	DQ37	257	VPP	82	VSS	170	DQ36	258	VTT
83	DQ26	171	VSS	259	VPP	84	DQ27	172	VSS	260	SA1
85	VSS	173	DQ33	-	-	86	VSS	174	DQ32	-	-
87	CB5/NC	175	VSS	-	-	88	CB4/NC	176	VSS	-	-

5.2.Pin Description

Pin Name	Description	Pin Name	Description
A0–A15	SDRAM address bus	CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)
BA0, BA1	SDRAM bank select		
BG0, BG1	SDRAM bank group select	PARITY	SDRAM parity input
RAS_n	SDRAM row address strobe	VDD	SDRAM I/O and core power supply
CAS_n	SDRAM column address strobe	VREFCA	SDRAM command/address reference supply
WE_n	SDRAM write enable	VSS	Power supply return (ground)
CS0_n, CS1_n CS2_n, CS3_n	DIMM Rank Select Lines	VDDSPD	Serial SPD EEPROM positive power supply
CKE0, CKE1	SDRAM clock enable lines	SCL	I2C serial bus clock for EEPROM
ODT0, ODT1	SDRAM on-die termination control lines	SDA	I2C serial bus data line for EEPROM
ACT_n	SDRAM activate	SA0–SA2	I2C slave address select for EEPROM
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
DM_n/DBI_n/	Input data mask and data bus inversion	RESET_n	Set DRAMs to a Known State
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	EVENT_n	SPD signals a thermal event has occurred
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	VTT	SDRAM I/O termination supply

6. ADVANTECH SDRAM Operation Condition

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1), 2)
V_{DDQ}	Supply Voltage	1.14	1.2	1.26	V	1), 2)
Single Ended AC/DC Input Levels						
$V_{IH\ (DC)}$	DC Input Logic High	V_{REF}+0.065	-	VDD	V	
$V_{IL\ (DC)}$	DC Input Logic Low	V_{SS}	-	VREF-0.065	V	
$V_{IH\ (AC)}$	AC Input Logic High	VREF+0.09	-	3)	V	
$V_{IL\ (AC)}$	AC Input Low (Logic0) Voltage	3)	-	VREF-0.09	V	
$V_{REFCA\ (DC)}$	I/O Reference Voltage	0.49*VDDQ	-	0.51*VDDQ	V	3),4)
Single Ended AC/DC output Levels						
$V_{OH\ (DC)}$	DC output high measurement level	-	1.1 x VDDQ	-	V	
$V_{OM\ (DC)}$	DC output mid measurement level	-	0.8 x VDDQ	-	V	
$V_{OL\ (DC)}$	DC output low measurement level	-	0.5 x VDDQ	-	V	
$V_{OH\ (AC)}$	AC output high measurement level	-	(0.7 + 0.15) x VDDQ	-	V	5)
$V_{OL\ (AC)}$	AC output low measurement level		(0.7 - 0.15) x VDDQ	-	V	5)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
$V_{IHdiff(DC)}$	Differential input high DC	+0.110	-	6)	V	7)
$V_{ILdiff(DC)}$	Differential input low DC	6)	-	-0.110	V	7)
$V_{IHdiff(ac)}$	Differential input high AC	2 x (VIH(AC) - VREF)	-	6)	V	8)
$V_{ILdiff(ac)}$	Differential input low AC	6)	-	2 x (VIL(AC) -VREF)	V	8)
Differential AC and DC Output Levels						
$V_{OHdiff(AC)}$	AC differential output high measurement level	-	0.3 x VDDQ	-	V	9)
$V_{OLdiff(AC)}$	AC differential output low measurement level	-	-0.3 x VDDQ	-	V	9)

Note:

1) Under all conditions VDDQ must be less than or equal to VDD.

2) VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.

3) The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference: approx. ± 12mV)

4) For reference: approx. VDD/2 ± 12mV

5) The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

6) These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (VIH.CA(DC) max, VIL.CA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

7) Used to define a differential signal slew-rate.

8) For CK_t - CK_c use VIH.CA/VIL.CA(AC) of ADD/CMD and VREFCA

9) The swing of ± 0.3 × VDDQ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ at each of the differential outputs.

7. Serial Presence Detect

- SQR-SD4N4G3K2MNPEA

Byte	Description	Value	Hex Value
0	Number of Serial PD Bytes Written / SPD Device Size	SPD bytes used: 512 bytes SPD bytes total: 512 bytes	24
1	SPD Revision	Revision 1.2	12
2	DRAM Device Type	DDR4 SDRAM	0C
3	Module Type	SO-DIMM	03
4	SDRAM Density and Banks	8 Gb, 8 banks	45
5	SDRAM Addressing	Row: 16, Column: 10	21
6	Primary SDRAM Package Type	Monolithic Single die Not specified	00
7	SDRAM Optional Features	Unlimited MAC	08
8	SDRAM Thermal and Refresh Options	Reserved	00
9	Other SDRAM Optional Features	Post package repair supported Soft PPR supported	60
10	Secondary SDRAM Package Type	-	00
11	Module Nominal Voltage, VDD	1.2V	03
12	Module Organization	1 Rank x 16 bits	02
13	Module Memory Bus Width	Non-ECC, 64 bits	03
14	Module Thermal Sensor	Not incorporated	00
15	Extended Module Type	Reserved	00
16	Reserved	-	00
17	Timebases	MTB = 125 ps FTB = 1 ps	00
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.625 ns	05
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.625 ns	0D
20-23	CAS Latencies Supported	10 11 12 13 14 15 16 17 18 19 20 22 24	F8 BF 02 00
24	Minimum CAS Latency Time (tAAmin)	13.75 ns	6E
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.75 ns	6E

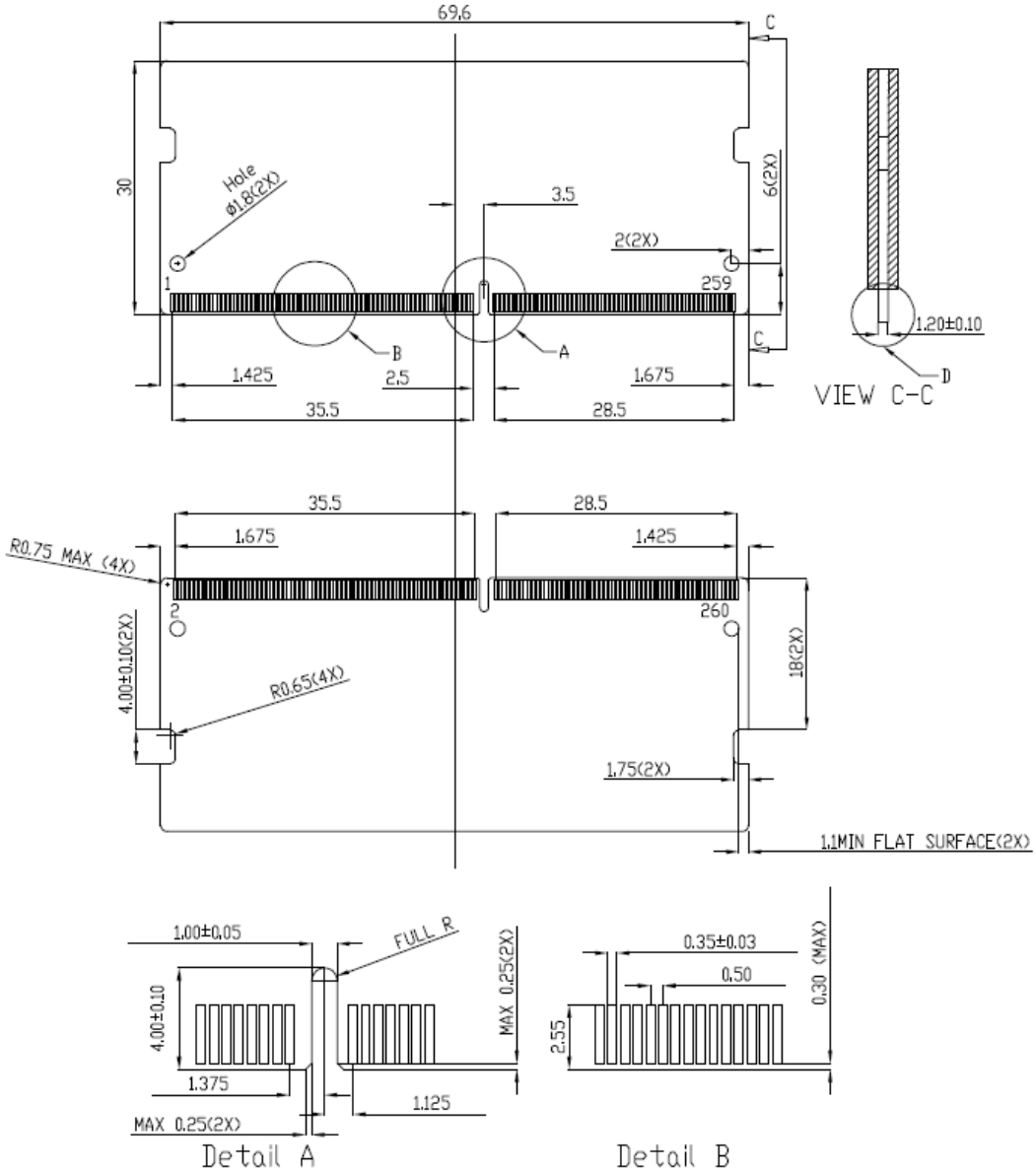
26	Minimum Row Precharge Delay Time (tRPmin)	13.75 ns	6E
27	Upper Nibbles for tRASmin and tRCmin	See bytes 28, 29	11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	32 ns	00
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	45.75 ns	6E
30-31	Minimum Refresh Recovery Delay Time (tRFC1min)	350 ns	F0 0A
32-33	Minimum Refresh Recovery Delay Time (tRFC2min)	260 ns	20 08
34-35	Minimum Refresh Recovery Delay Time (tRFC4min)	160 ns	00 05
36-37	Minimum Four Activate Window Delay Time (tFAWmin)	30 ns	00 F0
38	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	5.375 ns	2B
39	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	6.5 ns	34
40	Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	5 ns	28
41-42	Minimum Write Recovery Time(tWRmin)	15 ns	00 78
43	Upper Nibbles for tWTRmin	See bytes 44, 45	00
44	Minimum Write to Read Time(tWTR_Smin), different bank group	2.5 ns	14
45	Minimum Write to Read Time(tWTR_Lmin), same bank group	7.5 ns	3C
46-59	Reserved	-	00
60	Connector to SDRAM Bit Mapping for bits DQ0-3	3 1 2 0	16
61	Connector to SDRAM Bit Mapping for bits DQ4-7	7 5 6 4	36
62	Connector to SDRAM Bit Mapping for bits DQ8-11	1 3 0 2	0B
63	Connector to SDRAM Bit Mapping for bits DQ12-15	7 5 4 6	35
64	Connector to SDRAM Bit Mapping for bits DQ16-19	3 1 2 0	16
65	Connector to SDRAM Bit Mapping for bits DQ20-23	7 5 6 4	36
66	Connector to SDRAM Bit Mapping for bits DQ24-27	1 3 0 2	0B
67	Connector to SDRAM Bit Mapping for bits DQ28-31	7 5 4 6	35

68	Connector to SDRAM Bit Mapping for bits CB0-3	-	00
69	Connector to SDRAM Bit Mapping for bits CB4-7	-	00
70	Connector to SDRAM Bit Mapping for bits DQ32-35	3 1 2 0	16
71	Connector to SDRAM Bit Mapping for bits DQ36-39	7 5 6 4	36
72	Connector to SDRAM Bit Mapping for bits DQ40-43	1 3 0 2	0B
73	Connector to SDRAM Bit Mapping for bits DQ44-47	7 5 4 6	35
74	Connector to SDRAM Bit Mapping for bits DQ48-51	3 1 2 0	16
75	Connector to SDRAM Bit Mapping for bits DQ52-55	7 5 6 4	36
76	Connector to SDRAM Bit Mapping for bits DQ56-59	1 3 0 2	0B
77	Connector to SDRAM Bit Mapping for bits DQ60-63	7 5 4 6	35
78-116	Reserved	-	00
117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	0 ps	00
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	-100 ps	9C
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	-75 ps	B5
120	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	0 ps	00
121	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	0 ps	00
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCDmin)	0 ps	00
123	Fine Offset for Minimum CAS Latency Time (tAAmin)	0 ps	00
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVGmax)	-25 ps	E7
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVGmin)	0 ps	00
126-127	CRC for Base Configuration Section	CRC for bytes 0-125	89 59
128	Raw Card Extension, Module Nominal Height	29 < Height ≤ 30 mm	0F

129	Module Maximum Thickness	1 < Front ≤ 2 mm Back ≤ 1 mm	01
130	Reference Raw Card Used	R/C C0	02
131	Address Mapping from Edge Connector to DRAM	Standard	00
132-253	Reserved	-	00
254-255	Cyclical Redundancy Code (CRC) for SPD Block 1	CRC for bytes 128-253	C0 E2
256-319	Reserved	-	00
320-321	Module Manufacturer's ID Code	Advantech	8A C8
322	Module Manufacturing Location	Taipei	54
323-324	Module Manufacturing Date	Year, Week	Variable
325-328	Module Serial Number	By Manufacturer	Variable
329-348	Module Part Number	SQR-SD4N4G3K2MNPEA	53 51 52 2D 53 44 34 4E 34 47 33 4B 32 4D 4E 50 45 41 20 20
349	Module Revision Code	-	00
350-351	DRAM Manufacturer's ID Code	Micron	80 2C
352	DRAM Stepping	Stepping information not provided	Variable
353-381	Module Manufacturer's Specific Data	By Manufacturer	00
382-383	Reserved	-	00
384-511	End User Programmable	Reserved	00

8. Package Dimension

-4GB DDR4 SODIMM, 512Mx64, 1 Rank



Note : All dimensions are in millimeters[mils] and should be kept within a tolerance of ±0.15[6], unless otherwise specified.

9. Reliability Specifications

9.1.Environmental Conditions

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature	0 to +85	°C	1),2)
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	3)

Note:

1) Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

2) At 0° C - 85° C, operation temperature range are the temperature which all DRAM specification will be supported.

3) Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

10. Operating, Standby and Refresh Currents

- **4GB SODIMM** (1Rank 512Mx16 DDR4 SDRAMs)

Symbol	Parameter/Condition	PC4-25600	Unit
IDD0	Operating One bank Active-Precharge current	216	mA
IDD1	Operating One bank Active-read-Precharge current	320	mA
IDD2P	Precharge power-down current	88	mA
IDD2Q	Precharge quiet standby current	104	mA
IDD2N	Precharge standby current	132	mA
IDD3P	Active power - down current	136	mA
IDD3N	Active standby current	176	mA
IDD4R	Operating burst read current	1248	mA
IDD4W	Operating burst write current	1000	mA
IDD5	Burst refresh current	200	mA
IDD6	Self refresh current	136	mA
I DD7	Operating bank interleave read current	1080	mA