SODIMM DDR4 2400 8GB Datasheet

(SQR-SD4N8G2K4HNEBC)

Features:

- **Compliance with**
  - JEDEC Standard 260-pin small-outline dual in-line memory module
  - Intend for PC4-19200 application
  - Backward compatible with PC4-17000 and PC4-14900
  - Bi-Directional Differential Data Strobe
  - 8 Bit pre-fetch
  - 16 Internal banks
  - Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
  - Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
  - On-Die Termination (ODT)
  - On-Board EEPROM
  - Internal Vref DQ level generation is available
  - RoHS and Halogen free
  - Golden connector

- **Capacities**

  8GB 1Gbx64 2 rank

- **Performance**
  - DDR4-2400 PC4-19200 CL17
  - DDR4-2133 PC4-17000 CL15
  - DDR4-1866 PC4-14900 CL13

- **DRAM Type**
  - DDR4 SODIMM

- **Temperature ranges**

Operating:

  - Standard: 0°C to 85°C

Storage:

  - -50°C to 100°C

- **Supply voltage**
  - VDD=VDDQ=1.2 Volt (TYP)
  - VPP=2.5 Volt (TYP)
  - VDDSPD=2.25V~3.6V
- **Operation Current**
  - Active mode(max):
    8GB:1.56 A
    (TCASE: 0°C to 95°C)

- **Form factor**
  - DDR4 260pin SODIMM

- **Shock &Vibration**
  - Shock: 1000G@1ms
  - Vibration: 20 G

- **Certification and Compliance**
  - RoHs
  - REACH
  - CE
  - FCC

RevisionHistory:

Rev.	Description	Date
1.0	Official release	2019/03/04

CONTENTS

1. ADVANTECH Memory Product Description

1.1 Introduction

ADVANTECH Unbuffered Small Outline DDR4 SDRAM DIMMs (Unbuffered Small Outline Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These DDR4 SDRAM Unbuffered Small Outline DIMMs are intended for use as main memory when installed in systems such as micro servers and mobile personal computers.

1.2 Key Parameter

Industry Nomenclature	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
	CL=13	CL=15	CL=17			
PC4-2400	1866	2133	2400	14.06	14.06	47.06

1.3 Ordering Information

DDR4 SODIMM					
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank
SQR-SD4N8G2K4HNEBC	8GB	PC4-19200	1Gx64	16	2

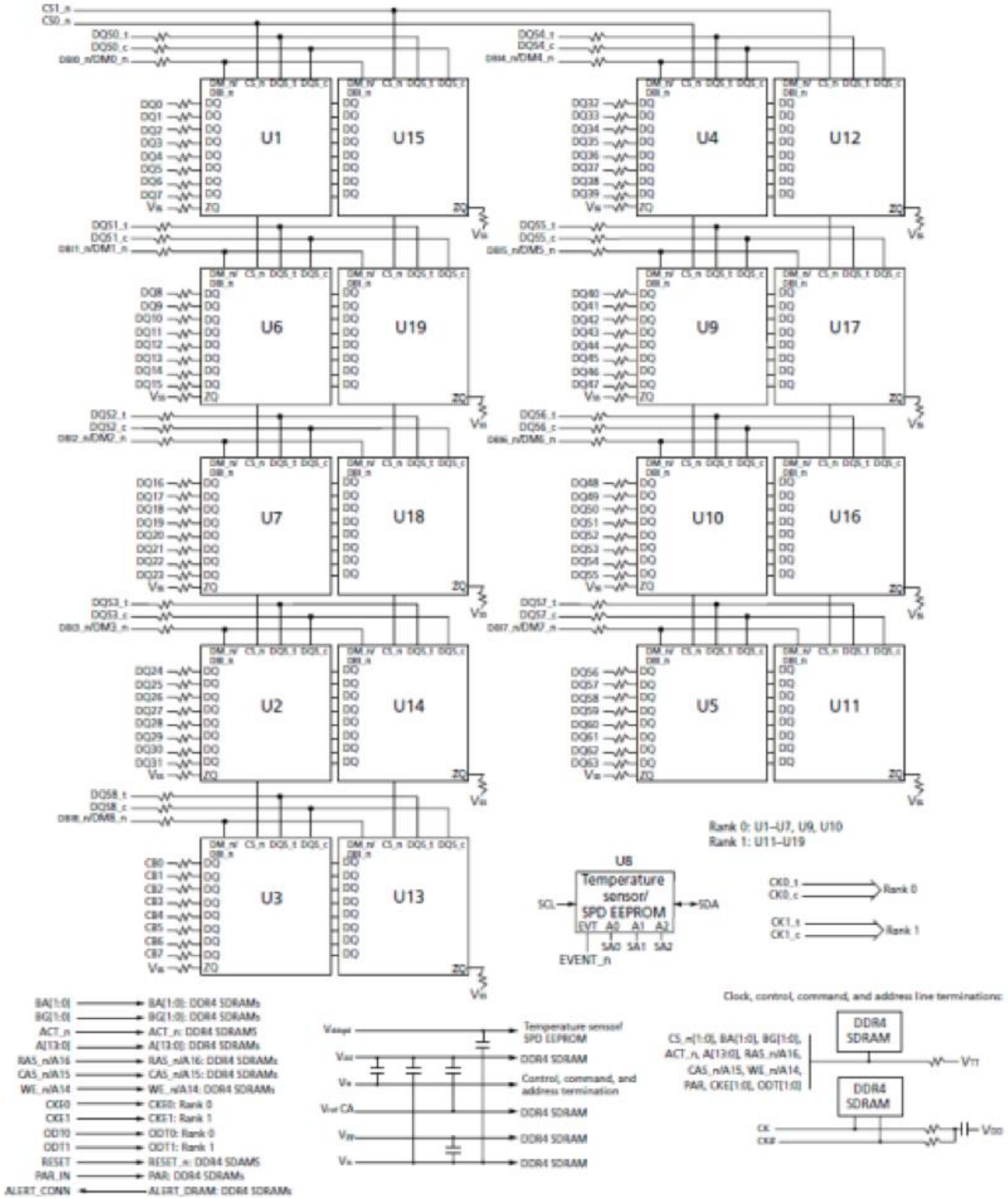
1.4 ADVANTECH Value Added Service

ADVANTECH DIMM provides specialized services to IPC designing customized hardware and systems by offering:

- Locked BOM control with customer product change notification(PCN)
- Pre-installed software, custom software imaging and ID strings
- Custom packaging and labeling
- Comprehensive supply-chain management
- Customer specified testing
- Localized Field Application Engineering for complete pre and post-sale technical support
- Optional Extend Temperature, ASTM B809-95 certified and conformal coating service.

2. ADVANTECH Memory Module Block Diagram

- DDR4,8GB, 512Mx8 base, 2Rank



Note:

- Unless otherwise noted, resistor value are 15Ω±5%
- ZQ resisters are 240Ω±1%. For all other resistor values refer to the appropriated wiring diagram
- To connector the SPDA2 input to the edge connector pin 166 install R1. To tie the SPD input A2 to ground install R2. Do not install both R1 and R2. The Value for R1 and R2 are not critical. Any value less than 100Ω may be used.

3. *Environment Requirement*

3.1.ADVANTECH DIMM Parameter

ADVANTECH DIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +65	°C	1
TSTG	Storage Temperature	-50 to +100	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	
PBAR	Barometric Pressure (operating& storage)	105 to 69	K Pascal	1,2
1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR4 DRAM component specification. 2. Up to 9850 ft.				

3.2.SDARM parameter by device density

RTT_Nom Setting	Parameter		4Gb	Units
tREFI	Average periodic refresh interval	0°C≦**TCASE**≦**85**°C	7.8	µs
		85°C≦**TCASE**≦**95**°C	3.9	µs

4. *Absolute Maximum Rating*

4.1.Module Absolut Maximum Rating

Symbol	**Parameter**	**Rating**	**Units**	**Notes**
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.4 to 1.5	V	
V_{DD}	Voltage on VDD supply relative to Vss	-0.4 to +1.5	V	1
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.4 to +1.5	V	1
V_{PP}	Voltage on VPP supply relative to Vss	-0.4 to +3.0	V	2

Note:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.

2. VPP must be greater than or equal to VDD at all times.

4.2.SDRAM Absolut Maximum Rating

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	℃	1,2
		Extended Temp.(optional)	85 to 95	℃	1,3
T_{STG}	Storage Temperature		-55 to 100	℃	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.3 to +1.5	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.3 to +1.5	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.3 to +1.5	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C underall operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 ℃ case temperature. Full specifications are supported in this range, but the following additionalconditions apply:
    a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
    b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurementconditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all timesand VREF must be not greater than0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

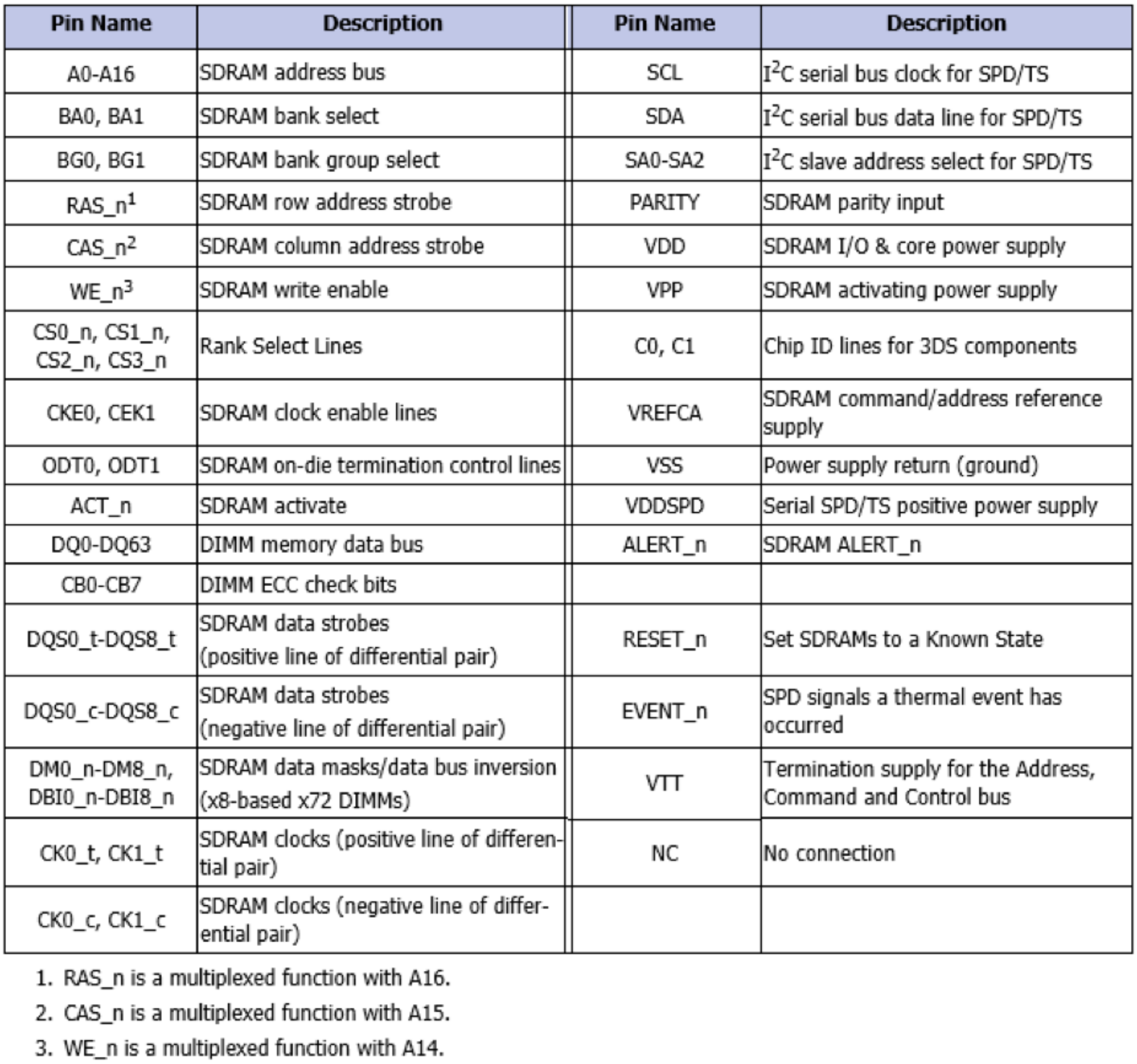
5. *Pin Configurations (Front side/Back side)*

5.1.DDR4 SODIMM Pin Assignment

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	67	DQ29	68	VSS	133	A1	134	EVENT_n, NF	199	DM5_n/DBI5_n	200	DQS5_t
3	DQ5	4	DQ4	69	VSS	70	DQ24	135	VDD	136	VDD	201	VSS	202	VSS
5	VSS	6	VSS	71	DQ25	72	VSS	137	CK0_t	138	CK1_t/NF	203	DQ46	204	DQ47
7	DQ1	8	DQ0	73	VSS	74	DQS3_c	139	CK0_c	140	CK1_c/NF	205	VSS	206	VSS
9	VSS	10	VSS	75	DM3_n/DMI3_n	76	DQS3_t	141	VDD	142	VDD	207	DQ42	208	DQ43
11	DQS0_c	12	DM0_n/DM10_n	77	VSS	78	VSS	143	PARITY	144	A0	209	VSS	210	VSS
13	DQS0_t	14	VSS	79	DQ30	80	DQ31	145	BA1	146	A10/AP	211	DQ52	212	DQ53
15	VSS	16	DQ6	81	VSS	82	VSS	147	VDD	148	VDD	213	VSS	214	VSS
17	DQ7	18	VSS	83	DQ26	84	DQ27	149	CS0_n	150	BA0	215	DQ49	216	DQ48
19	VSS	20	DQ2	85	VSS	86	VSS	151	WE_n/A14	152	RAS_n/A16	217	VSS	218	VSS
21	DQ3	22	VSS	87	CB5/NC	88	CB4/NC	153	VDD	154	VDD	219	DQS6_c	220	DM6_n/DBI6_n
23	VSS	24	DQ12	89	VSS	90	VSS	155	ODT0	156	CAS_n/A15	221	DQS6_t	222	VSS
25	DQ13	26	VSS	91	CB1/NC	92	CB0/NC	157	CS1_n	158	A13	223	VSS	224	DQ54
27	VSS	28	DQ8	93	VSS	94	VSS	159	VDD	160	VDD	225	DQ55	226	VSS
29	DQ9	30	VSS	95	DQS8_c	96	DM8_n/DBI_n/NC	161	ODT1	162	C0/CS2_n/NC	227	VSS	228	DQ50
31	VSS	32	DQS1_c	97	DQS8_t	98	VSS	163	VDD	164	VREFCA	229	DQ51	230	VSS
33	DM1_n/DBI_n	34	DQS1_t	99	VSS	100	CB6/NC	165	C1, CS3_n, NC	166	SA2	231	VSS	232	DQ60
35	VSS	36	VSS	101	CB2/NC	102	VSS	167	VSS	168	VSS	233	DQ61	234	VSS
37	DQ15	38	DQ14	103	VSS	104	CB7/NC	169	DQ37	170	DQ36	235	VSS	236	DQ57
39	VSS	40	VSS	105	CB3/NC	106	VSS	171	VSS	172	VSS	237	DQ56	238	VSS
41	DQ10	42	DQ11	107	VSS	108	RESET_n	173	DQ33	174	DQ32	239	VSS	240	DQS7_c
43	VSS	44	VSS	109	CKE0	110	CKE1	175	VSS	176	VSS	241	DM7_n/DBI7_n	242	DQS7_t
45	DQ21	46	DQ20	111	VDD	112	VDD	177	DQS4_c	178	DM4_n/DBI4_n	243	VSS	244	VSS
47	VSS	48	VSS	113	BG1	114	ACT_n	179	DQS4_t	180	VSS	245	DQ62	246	DQ63
49	DQ17	50	DQ16	115	BG0	116	ALERT_n	181	VSS	182	DQ39	247	VSS	248	VSS
51	VSS	52	VSS	117	VDD	118	VDD	183	DQ38	184	VSS	249	DQ58	250	DQ59
53	DQS2_c	54	DM2_n/DBI2_n	119	A12	120	A11	185	VSS	186	DQ35	251	VSS	252	VSS
55	DQS2_t	56	VSS	121	A9	122	A7	187	DQ34	188	VSS	253	SCL	254	SDA
57	VSS	58	DQ22	123	VDD	124	VDD	189	VSS	190	DQ45	255	VDDSPD	256	SA0
59	DQ23	60	VSS	125	A8	126	A5	191	DQ44	192	VSS	257	VPP	258	VTT
61	VSS	62	DQ18	127	A6	128	A4	193	VSS	194	DQ41	259	VPP	260	SA1
63	DQ19	64	VSS	129	VDD	130	VDD	195	DQ40	196	VSS				
65	VSS	66	DQ28	131	A3	132	A2	197	VSS	198	DQS5_c				

Note:
1. NC = No Connect, RFU = Reserved for Future Use
2. Address A17 is only valid for 16 Gb x4 based SDRAMs.
3. RAS_n is a multiplexed function with A16.
4. CAS_n is a multiplexed function with A15.
5. WE_n is a multiplexed function with A14.
6. CBx are available for ECC function

5.2.Pin Description



Pin Name	Description	Pin Name	Description
A0-A16	SDRAM address bus	SCL	I^2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I^2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0-SA2	I^2C slave address select for SPD/TS
RAS_n[1]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[2]	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n[3]	SDRAM write enable	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	Rank Select Lines	C0, C1	Chip ID lines for 3DS components
CKE0, CEK1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0-CB7	DIMM ECC check bits		
DQS0_t-DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c-DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred
DM0_n-DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	VTT	Termination supply for the Address, Command and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

1. RAS_n is a multiplexed function with A16.
2. CAS_n is a multiplexed function with A15.
3. WE_n is a multiplexed function with A14.

6. ADVANTECH SDRAM Operation Condition

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage command/address bus	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	3
I_{VTT}	Termination reference voltage (DC) –command/address bus	-750	-	750	mA	
V_{TT}	Termination Voltage	0.49 × VDD - 20mV	0.5 × VDD	0.51 × VDD + 20mV	V	4
I_{I}	Input leakage current; any input excluding ZQ; 0V < VIN < 1.1V	-2.0	-	2.0	µA	5
II/O	DQ leakage; 0V < Vin < VDD	-4.0	-	4.0	µA	5
I_{OZpd}	Output leakage current; VOUT = VDD; DQ is disabled	-	-	5.0	µA	5,6
I_{OZpu}	Output leakage current; VOUT =VSS; DQ and ODT are disabled; ODT is disabled with ODT input HIGH	V_{REF} + 0.125	-	V_{DDQ} + 0.3	µA	1
I_{OZpd}	VREFCA leakage; VREFCA = VDD/2 (after DRAM is initialized)	-2.0	-	2.0	µA	5

Note:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
5. Multiply by the number of DRAM die on the module.
6. Tied to ground. Not connected to edge connector.

7. Operating, Standby and Refresh Currents

- **8GB SODIMM** (2Rank 512Mx8 DDR4 SDRAMs)

- **Symbol**	**Proposed Conditions**	**Value**		**Units**
		IDD Max.	**IPP Max.**	
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	470	63	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	505	63	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODTSignal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	575	63	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	603	63	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	325	54	mA

IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	395	54	mA
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to ComponentDatasheet for detail pattern	350	54	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	305	54	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	350	54	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	305	54	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	350	54	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	205	54	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	315	54	mA
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1;	450	54	mA

	Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern			

IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	495	54	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	295	54	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1100	54	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	1135	54	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	1125	54	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	900	54	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	945	54	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	900	54	mA

IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	830	54	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	945	54	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1565	189	mA
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	1315	162	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	1035	126	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	225	72	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	295	72	mA

IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	170	54	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	225	72	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1035	95	mA
IDD8	Maximum Power Down Current TBD	145	36	mA

8. Serial Presence Detect

- *SQR-SD4N8G2K4HNEBC*

Byte	Description	Function support	Byte Value (Hexadecimal)
0	SPD BYTES USE/TOTAL BYTES AVAILABLE/CRC COVERAGE	SPD Bytes Used : 384 / SPD Bytes Total : 512	23
1	SPD REVISION	Rev 1.1	11
2	DRAM DEVICE TYPE	DDR4 SDRAM	0C
3	MODULE TYPE (FORM FACTOR)	nECC SO-DIMM	03
4	SDRAM DEVICE DENSITY BANKS	4GB/4BK/4Gb	84
5	SDRAM DEVICE ADDRESSING	15/10	19
6	SDRAM DEVICE TYPE (ARCHITECURE)	SDP	00
7	SDRAM DEVICE OPTIONAL FEATURES	Unlimited MAC	08
8	SDRAM DEVICE THERMAL REFRESH OPTIONS	Reserved	00
9	OTHER SDRAM OPTIONAL FEATURES	hPPR supported	40
10	SECONDARY SDRAM PACKAGE TYPE	Blank	00
11	NOMINAL MODULE VOLTAGE (VDD)	1.2V	03
12	MODULE ORG. (PACKAGE RANKS DEVICE WIDTH)	2Rx8	09
13	MODULE MEMORY BUS WIDTH	LP/x64	03
14	MODULE THERMAL SENSOR SUPPORT	Thermal sensor supported	80
15	EXTENDED MODULE TYPE	Blank	00
16	BYTE 16 RESERVED	Blank	00
17	TIMEBASES (MTB FTB)	MTB : 125ps, FTB : 1ps	00
18	SDRAM DEVICE TCKMIN	0.833ns	07
19	SDRM DEVICE TCKMAX	1.6ns	0D
20	CL7 THROUGH CL14 SUPPORT	14, 13, 12, 11, 9	F8
21	CL15 THROUGH CL22 SUPPORT	16, 15	0F
22	CL23 THROUGH CL30 SUPPORT		00
23	CL31 THROUGH CL36 SUPPORT-CL RNG		00

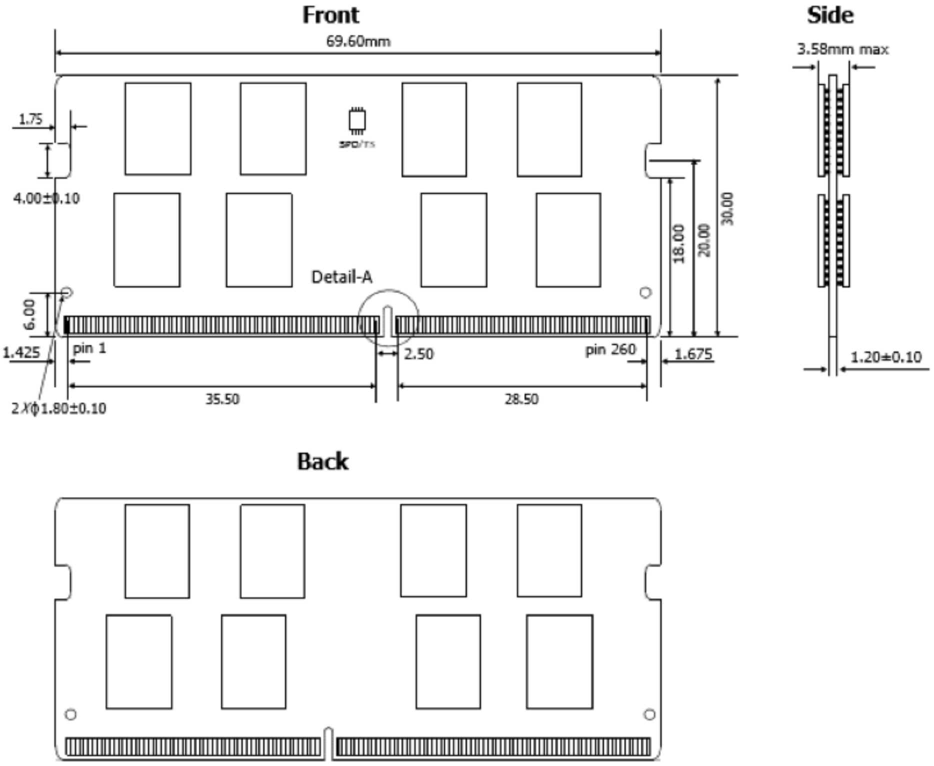
24	MIN CAS LATENCY (TAAMIN)	13.75ns	6E
25	MIN RAS TO CAS DELAY (TRCDMIN)	13.75ns	6E
26	MIN ROW PRECHARGE DELAY (TRPMIN)	13.75ns	6E
27	UPPER NIBBLE TRASMIN, TRCMIN	33ns / 46.50ns	11
28	MIN ACTIVE TO PRECHARGE DELAY (TRASMIN) LSB	33ns	00
29	MIN ACTIVE TO ACTIVE/REFRESH DELAY (TRCMIN) LSB	46.50ns	6E
30	MIN REFRESH RECOVERY DELAY (TRFC1MIN) LSB	260ns	20
31	MIN REFRESH RECOVERY DELAY (TRFC1MIN) MSB	260ns	08
32	MIN REFRESH RECOVERY TIME DELAY (TRFC2MIN) LSB	160ns	00
33	MIN REFRESH RECOVERY DELAY (TRFC2MIN) MSB	160ns	05
34	DDR4-MIN REFRESH RECOVERY DELAY (TRFC4MIN) LSB	110ns	70
35	MIN REFRESH RECOVERY DELAY (TRFC4MIN) MSB	110ns	03
36	MIN FOUR ACTIVE WINDOW DELAY (TFAWMIN) UPPER NIB	21ns	00
37	MIN FOUR ACTIVE WINDOW DELAY (TFAWMIN) LSB	21ns	A8
38	MIN ACTIVE TO ACTIVE DELAY (TRRD_SMIN) DIFRNT BANK GRP	3.7ns	1B
39	MIN ACTIVE TO ACTIVE DELAY (TRRD_LMIN) SAME BANK GRP	5.30ns	28
40	MIN CAS TO CAS DELAY, SAME BG (TCCDLMIN)	5.628ns	28
41	TWRMIN MSB	15ns	00
42	TWRMIN LSB	15ns	78
43	TWTR_LMIN/TWTR_SMIN - MSB (UPPER NIBLS)	2.5ns/7.5ns	00
44	TWTR_SMIN - LSB	2.5ns	14
45	TWTR_LMIN - LSB	7.5ns	3C
46-59	RESERVED BYTES 46 - 59	Blank	00
60	DDR4-BIT MAP, DQ0 - 3	DQ0-3	0B
61	DDR4-BIT MAP, DQ4 -7	DQ4-7	2B
62	DDR4-BIT MAP, DQ8 - 11	DQ8-11	0C
63	DDR4-BIT MAP, DQ12 - 15	DQ12-15	2B

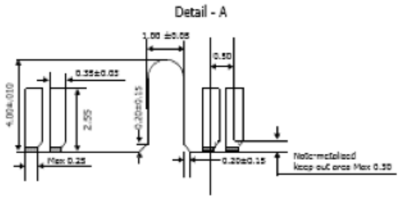
64	DDR4-BIT MAP, DQ16 - 19	DQ16-19	2B
65	DDR4-BIT MAP, DQ20 - 23	DQ20-23	0B
66	DDR4-BIT MAP, DQ24 - 27	DQ24-27	16
67	DDR4-BIT MAP, DQ28 - 31	DQ28-31	36
68	DDR4-BIT MAP, CB0 - 3	CB0-3	00
69	DDR4-BIT MAP, CB4 - 7	CB4-7	00
70	DDR4-BIT MAP, DQ32 - 35	DQ32-35	15
71	DDR4-BIT MAP, DQ36 - 39	DQ36-39	2C
72	DDR4-BIT MAP, DQ40 - 43	DQ40-43	0B
73	DDR4-BIT MAP, DQ44 - 47	DQ44-47	35
74	DDR4-BIT MAP, DQ48 - 51	DQ48-51	16
75	DDR4-BIT MAP, DQ52 - 55	DQ52-55	36
76	DDR4-BIT MAP, DQ56 - 59	DQ56-59	16
77	DDR4-BIT MAP, DQ60 - 63	DQ60-63	36
78-116	RESERVE BYTES 78 - 116	Blank	00
117	FTB OFFSET - TCCDLMIN	5.628ns	00
118	FTB OFFSET - TRRD_LMIN	5.30ns	9C
119	FTB OFFSET - TRRD_SMIN	3.7ns	B5
120	FTB OFFSET - TRCMIN	46.50ns	00
121	FTB OFFSET - TRPMIN	13.50ns	00
122	FTB OFFSET - TRCDMIN	13.50ns	00
123	FTB OFFSET - TAAMIN	13.50ns	00
124	FTB OFFSET - TCKMAX	1.6ns	E7
125	FTB OFFSET - TCKMIN	0.833ns	D6
126-127	CRC FOR BYTES 0 - 125, BASE CONFIG	CRC cover 0~125 byte	D4 DD
128	RAW CARD EXT. AND MODULE NOM. HEIGHT	30.00	0F
129	MODULE MAX THICKNESS	1.2/1.2	11
130	RAW CARD ID	E0	04
131	UDIMM ADDRESS MAPPING - RDIMM MODULE ATTRIBUTES	Mirrored	01

132	RDIMM HEAT SPREADER SOLUTION	Blank	00
133	RDIMM REGISER MFR. ID (LSB)	Blank	00
134	REGISTER MFR. ID (MSB)	Blank	00
135	REGISTER REVISION NUMBER	Blank	00
136	REGISTER ADDRESS MAPPING	Blank	00
137	REG OUTPUT DRIVE FOR CONTROL	Blank	00
138	REG OUTPUT DRIVE FOR CLOCK	Blank	00
139-253	RESERVE BYTES 139 - 253	Blank	00
254-255	CRC FOR MODULE SPECIFIC BYTES 128-253	CRC cover 128~253 byte	FF DB
256-319	BYTES 256 - 319 RESERVED	Blank	00
320	MODULE MFR. ID CODE (LSB)	ADVANTECH JEDEC ID	8A
321	MODULE MFR. ID COD (MSB)	ADVANTECH JEDEC ID	C8
322	MODULE MFR. LOCATION	Taiwan	02
323-324	MODULE MFR. DATE	-	-
325-328	MODULE SERIAL NUMBER	-	-
329-348	MODULE PART NUMBER	SQR-SD4N8G2K4HNEBC	53 51 52 2D 53 44 34 4E 38 47 32 4B 34 48 4E 45 42 43
349	MODULE PCB REV	0	00
350	DRAM MFR. ID CODE (LSB)	SK hynix	80
351	DRAM MFR. ID CODE (MSB)	SK hynix	AD
352	DEVICE DIE REV (PART MARKING)	Undefined	FF
353-383	BYTES 353 - 383 RESERVED	-	-
384-511	BYTES 384-511 END USER RESERVED	Blank	00

9. Package Dimension

-8GB DDR4 SODIMM, 512Mx64, 2 Rank





Note:

1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

2. The dimensional diagram is for reference only.

10. Reliability Specifications

10.1. Environmental Conditions

Environmental specifications are following MIL-STD-810F, as below table.

Environment	Specification
Storage Temperature	-50°C ~ +100°C
Operating Temperature	0°C to 85°C (Standard)
Vibration	20G
Shock	1000G@1ms